

**REMARKS**

Claims 1-26 and 40-67 are currently pending in this application. By this Amendment claims 1, 13, 14, 26, 40, 43, 45, 46, 48-51, 53, 54, 57, 59, 60, 62-65 and 67 are amended. Support for the amendments is found in the specification, including the claims, as filed. No new matter has been introduced. Favorable reconsideration of the application in light of the foregoing amendments and following comments is respectfully solicited.

In section 2 of the Office Action, claims 1-10, 13-23 and 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lahti (U.S. Patent No. 4,875,161).

In section 3 of the Office Action, claims 1, 11, 12, 14, 24 and 25 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lee (U.S. Patent No. 6,381,690).

In section 4 of the Office Action, claims 40-47, 49, 50, 54-61, 63 and 64 were rejected under 35 U.S.C. § 102(b) as being anticipated by Cray (U.S. Patent No. 4,128,880).

In section 5 of the Office Action, claims 12 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Matsuura (U.S. Patent No. 4,725,973).

In section 6 of the Office Action, claims 40, 48, 50-53, 54, 62 and 64-67 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Blleloch (Vector Models for Data-Parallel Computing) in view of *In re Rose*, 105 USPQ 237 (CCPA 1955).

Applicants respectfully traverse.

**I. LAHTI**

Claims 1-10, 13-23 and 26 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by Lahti (U.S. Patent No. 4,875,161). In order to expedite prosecution of this application, Applicants have amended independent claims 1, 13, 14 and 26 to recite:

the data selection operand comprising a plurality of fields each independently selecting one of the plurality of data elements (*emphasis showing amendment*)

The Office Action has provided indications that such an amendment would distinguish the invention from Lahti. Specifically, in response to Applicants' extensive prior arguments setting forth the significant differences between the present invention and the single address format taught by Lahti, the Office Action argued that without language to restrict the claims to either "individually" or "independently" selecting one of the plurality of data elements, the claims can be broadly construed to cover the Lahti system. The Office Action states:

Regarding the arguments directed to the limitation 'each selecting one of the plurality of data elements,' Examiner disagrees. Nowhere in the prior Office Action is it stated that individual fields used individually to select a word from Lahti's memory space. In fact, each field together MUST be used (as admitted by applicant) to "provide[e] the data element selected by the field." (*emphasis added*). Office Action dated August 8, 2008, p. 15, last paragraph.

Again, the claim does not require that each field have enough bits to independently select any element . . . (*emphasis added*). Office Action dated August 8, 2008, p. 16, second paragraph

Accordingly, Applicants have amended the claims to explicitly incorporate the language of "independently" as provided by the Office Action, to overcome the rejection based on Lahti.<sup>1</sup> Thus, amended claims 1, 13, 14 and 26 overcome the rejection. Claims 2-10 and 15-23, which depend from claims 1 and 14, respectively, and incorporate the limitations thereof, also overcome the rejection for at least the same reasons as stated above. Accordingly, Applicants respectfully request withdrawal of the anticipation rejection based on Lahti.

---

<sup>1</sup> While Applicants disagree with PTO's position that, prior to this amendment, the claims could be read broadly to encompass the Lahti system, Applicants have amended the claims in a manner suggested by the Office Action, in order to expedite prosecution of this application.

## II. LEE

Claims 1, 11, 12, 14, 24 and 25 were rejected under 35 U.S.C. § 102(e) as purportedly anticipated by Lee (U.S. Patent No. 6,381,690).

### A. Lee is Not Prior Art to the Present Application

Title 37 of the Code of Federal Regulations, section 1.131 provides that:

(a) When any claim of an application or a patent under reexamination is rejected, the inventor of the subject matter of the rejected claim, the owner of the patent under reexamination, or the party qualified under §§ 1.42, 1.43, or 1.47, may submit an appropriate oath or declaration to establish invention of the subject matter of the rejected claim prior to the effective date of the reference or activity on which the rejection is based . . .

(b) The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application. Original exhibits of drawings or records, or photocopies thereof, must accompany and form part of the affidavit or declaration or their absence must be satisfactorily explained.

The Lee patent has a filing date of August 1, 1995. The effective filing date of the present application is August 16, 1995, merely fifteen days after Lee's filing date.<sup>2</sup> Applicants submit that the present invention was conceived prior to the filing date of the Lee patent. Applicants further submit that due diligence was exercised to reduce the invention to practice from prior to the filing date of the Lee patent to the effective filing date of the present application, which represents constructive reduction to practice of the invention.<sup>3</sup>

---

<sup>2</sup> The present application is a continuation of U.S. patent application Ser. No. 10/646,787, filed Aug. 25, 2003, which is a continuation of U.S. patent application Ser. No. 09/922,319, filed Aug. 2, 2001, which is a continuation of U.S. patent application Ser. No. 09/382,402, filed Aug. 24, 1999, now U.S. Pat. No. 6,295,599, which claims the benefit of priority to Provisional Application No. 60/097,635 filed Aug. 24, 1998, and is a continuation-in-part of U.S. patent application Ser. No. 09/169,963, filed Oct. 13, 1998, now U.S. Pat. No. 6,006,318, which is a continuation of U.S. patent application Ser. No. 08/754,827, filed Nov. 22, 1996 now U.S. Pat. No. 5,822,603, which is a divisional of U.S. patent application Ser. No. 08/516,036, filed Aug. 16, 1995 now U.S. Pat. No. 5,742,840.

<sup>3</sup> The Applicants' reliance on constructive, rather than actual, reduction to practice should not be construed as an admission that no actual reduction to practice occurred.

Accordingly, Applicants herewith submit declarations under Rule 131 from Mr. Craig Hansen and Dr. John Moussouris, the inventors of the present application. These declarations are submitted along with their accompanying Exhibits 1-6, which provide factual evidence of conception prior to August 1, 1995 (filing date of the Lee patent), as well as factual evidence that the inventors (and their colleagues) exercised due diligence from just prior to August 1, 1995, through August 16, 1995, the date the invention was constructively reduced to practice by filing U.S. Patent Application Serial number 08/516,036, from which the present application claims priority.

**B. Evidence of Conception Prior to August 1, 1995**

Conception evidence and activities occurring prior to August 1, 1995, are described in detail in paragraphs 6-15 of Mr. Hansen's declaration and paragraphs 8-14 of Dr. Moussouris' declaration, and accordingly, will not be repeated here. Exhibits 1-2 of the declarations corroborate these activities and events and make clear that the inventors spent extensive time and effort conceiving and documenting their conception prior to August 1, 1995. The table below summarizes where the conception evidence is found in the declaration of Mr. Hansen:

CLAIM	CLAIM TERM	SUPPORT IN HANSEN DECLARATION
1	Processing data in a programmable processor	Paragraph 11 addresses support for this claim term.
14	Instruct a computer system to perform operations	Paragraph 11 addresses support for this claim term.
1, 14	decoding a single (group element selection) instruction for selectively arranging data specifying a data selection operand and a first and a second register each having a register width	Paragraph 12 discusses the G.SELECT.8 instruction and addresses support for this claim term.
1, 14	the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width	Paragraph 12 addresses support for this claim term.

CLAIM	CLAIM TERM	SUPPORT IN HANSEN DECLARATION
1, 14	the data selection operand comprising a plurality of fields each independently selecting one of the plurality of data elements	Paragraph 12 addresses support for this claim term.
1, 14	for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result	Paragraph 12 addresses support for this claim term.
1, 14	for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result	Paragraph 13 addresses support for this claim term.
11, 24	decoding a second single (group floating point multiply) instruction (for multiplying floating point data in a programmable processor) specifying a third and a fourth register each containing a plurality of floating-point operands	Paragraph 14 discusses instructions such as the GF.MUL.16, GF.MUL.32 and GF.MUL.64 instruction and addresses support for this claim term.
12, 25	multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products	Paragraph 14 addresses support for this claim term.
12, 25	providing the plurality of products to partitioned fields of a result register as a catenated result	Paragraph 14 addresses support for this claim term.

**C. Evidence of Due Diligence from Just Prior to August 1, 1995, through August 16, 1995**

Evidence of due diligence from just prior to August 1, 1995 through August 16, 1995 is described in detail in paragraphs 16-26 of Mr. Hansen's declaration and paragraphs 15-20 of Dr. Moussouris' declaration, and accordingly will not be repeated here. Exhibits 3, 4A-4D, 5 and 6 of the declarations corroborate the relevant activities and events starting just prior to August 1, 1995. As shown by these exhibits and the declaration evidence, the inventors and their colleagues spent considerable time reducing the invention to practice up until the constructive

reduction to practice of the present application on August 16, 1995. In particular, the voluminous diligence exhibits show the following activities occurred during the critical period:

- MicroUnity retained a team of patent prosecution attorneys from prior to August 1, 1995, through August 16, 1995, and this team of patent prosecution attorneys worked diligently with the inventors to prepare, finalize and file the very detailed '036 patent application, which was filed on August 16, 1995.<sup>4</sup> (*See* Exhibit 3 of the declarations).
- The individuals on the MicroUnity design team<sup>5</sup> spent substantial effort, in the time period from prior to August 1, 1995, through August 16, 1995, to build elaborate databases (sometimes called "tapeouts" or "physical layouts") for the invention disclosed in the '925 application. Exhibits 4A-4D of the declarations represent weekly logs of modifications to the electronic databases from August 1, 1995, through August 16, 1995. In the just the short span of time illustrated by Exhibits 4A-4D, there were approximately 129 changes to the electronic databases.
- Further evidence of MicroUnity's efforts to implement the invention of the '925 application in integrated circuit form is shown in email communications among the members of MicroUnity's design team from the time just prior to August 1, 1995, through August 16, 1995. The emails reflect the continual work performed

---

<sup>4</sup> The case law and MPEP guidance are clear that an applicant can rely on reasonable diligence in preparing and filing a patent application, in combination with reasonable diligence in working toward an actual reduction to practice. *Kondo v Martel*, 223 USPQ 528, 532 (Board of Patent Appeals 1984)("[A]ctivities directed toward an actual reduction to practice may be considered in conjunction with activities directed toward a constructive reduction to practice in order to show reasonably continuous diligence during the critical period.") (citing *ReyBellet v Engelhardt v Schindler*, 492 F.2d 1380 (C.C.P.A. 1974) for the proposition that "activity directed toward an actual reduction to practice followed by activity by an attorney culminating in the filing of a patent application established the requisite diligence during the critical period"); MPEP 2138.06 ("The diligence of attorney in preparing and filing patent application inures to the benefit of the inventor.").

<sup>5</sup> The MicroUnity design team included approximately 35 individuals, as shown by Exhibit 6 of the declarations.

by the MicroUnity design team during this time period to implement the invention in integrated circuit form. These emails are grouped and attached as Exhibit 5 to the declarations.

- Exhibit 6 of the declarations reflects various MicroUnity payroll records from prior to August 1, 2005 through August 16, 1995. This Exhibit shows that MicroUnity spent approximately \$138,000 to \$139,000 per pay period from just prior to August 1, 1995 through August 16, 1995.

As can be appreciated from inspection of Exhibits 3, 4A-4D, 5 and 6, the above list of due diligence activities during the critical period is by no means exhaustive, and accordingly, the Examiner is invited to review the detailed evidence in the declarations and attached exhibits.

Applicants respectfully submit that the declarations of Mr. Hansen and Dr. Moussouris show conception of at least claims 1, 11, 12, 14, 24 and 25 prior to the effective filing date of the Lee patent as well as the requisite level of due diligence during the critical period. For at least the reasons stated above, the Lee patent is not prior art to the present application.<sup>6</sup> Accordingly, Applicants request withdrawal of the anticipation rejection of claims 1, 11, 12, 14, 24 and 25 based on the Lee patent.

### **III. CRAY**

Claims 40-47, 49, 50, 54-61, 63 and 64 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by Cray (U.S. Patent No. 4,128,880). Claims 40 and 54 have been amended to recite, *inter alia*:

---

<sup>6</sup> Applicants reserve the right to distinguish over the Lee patent if the PTO does not accept the as persuasive the evidence presented in the Rule 131 declarations.

wherein each index in the index vector comprises a sufficient number of bits to represent a range of possible index values, the range of possible index values including a different index value for each of the plurality of data elements stored in the plurality of registers, allowing the index to select any data element from the plurality of data elements stored in the plurality of registers

Claims 50 and 64 have been amended to recite, *inter alia*:

wherein each index in the index vector comprises a sufficient number of bits to represent a range of possible index values, the range of possible index values including a different index value for each of the first and second pluralities of data elements stored in the first and second pluralities of registers, allowing the index to select any data element from the first and second pluralities of data elements stored in the plurality of registers

Cray fails to disclose the provision of data elements at predetermined positions through the use of an index vector such that each index in the index vector has a sufficient number of bits to represent a range of possible values that include a different index value for each of the data elements stored in a plurality of registers, to allow the index to select any data element from the plurality of data elements stored in the plurality of registers, as recited in these claims. Cray discloses a "merge" operation to merge two vectors  $V_j$  and  $V_k$ , under the control of a mask, to generate a result vector. This "merge" operation does not allow any re-ordering of the elements of either the  $V_j$  or  $V_k$  vector. Instead, the result vector maintains the order of the elements as they exist in vectors  $V_j$  and  $V_k$ . Specifically, the  $n$ th element of the result vector must be either the  $n$ th element of the  $V_j$  vector or the  $n$ th element of the  $V_k$  vector. Given the nature of such an operation, Cray only needs to make a binary decision – whether the data element in question should come from the  $V_j$  vector or the  $V_k$  vector. Accordingly, each selector found in Cray's mask is only a one-bit selector, not an index having sufficient number of bits to represent a full range of index values including a different index value for each of the elements of the vectors  $V_j$  and  $V_k$ .



Indeed, Cray teaches away from the index of the present invention that allows re-ordering of the data elements, because Cray's "merge" operation requires that the ordering of the elements remain fixed (the  $n$ th element of the result must be either the  $n$ th element of the  $V_j$  vector or the  $n$ th element of the  $V_k$  vector). Accordingly, Cray fails to disclose the provision of data elements at predetermined positions through the use of an index vector such that each index in the index vector has a sufficient number of bits to represent a range of possible values that include a different index value for each of the data elements stored in a plurality of registers, to allow the index to select any data element from the plurality of data elements stored in the plurality of registers, as recited in claims 40, 50, 54 and 64.

In view of the above, Applicants assert that the anticipation rejection of claims 40, 50, 54 and 64 based on Cray cannot stand and should be withdrawn. Claims 41-47 and 49 depend from claim 40 and incorporate all of its limitations. As such, Applicants submit that the anticipation rejection of claims 41-47 and 49 should be withdrawn for at least the reasons stated above with respect to claim 40. Claims 55-61 and 63 depend from claim 54 and incorporate all of its limitations. Applicants thus submit that the anticipation rejection of claims 55-61 and 63 should be withdrawn for at least the reasons stated above with respect to claim 54.

#### **IV. LEE IN VIEW OF MATSUURA**

Claims 12 and 25 were rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over Lee in view of Matsuura (U.S. Patent No. 4,725,973). As discussed in section II above, the Lee patent does not qualify as prior art with respect to the present application. Applicants have submitted herewith declarations of the inventors under 37 C.F.R. § 1.131 swearing behind the Lee patent. For at least this reason, the rejection of claims 12 and 25 under

§ 103 based on Lee in view of Matsuura cannot stand, and Applicants respectfully request withdrawal of the rejection.

#### V. BLELLOCH IN VIEW OF *IN RE ROSE*

Claims 40, 48, 50-53, 54, 62 and 64-67 were rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over Blelloch (Vector Models for Data-Parallel Computing) in view of *In re Rose*, 105 USPQ 237 (CCPA 1955). Claims 40 and 54 have been amended to recite, *inter alia*:

wherein each index in the index vector independently selects one of the data elements from the plurality of data elements stored in the plurality of registers; and for each index in the index vector, providing a data element selected by the index to a predetermined position in the destination register. (*emphasis added*)

Claims 50 and 64 have been amended to recite:

wherein each index in the index vector independently selects one of the data elements from the first and second pluralities of data elements stored in the first and second pluralities of registers; and for each index in the index vector,...provid[ing] a data element from one of the first or second plurality of data elements selected by the index to a predetermined position in the destination register, wherein the predetermined positions are contiguous blocks of bits that take up an entire width of the destination register. (*emphasis added*)

Even if Blelloch were combined with the principles of *In re Rose* (holding relating to changes in size), the resulting combination would not contain all of the features of claims 40, 50, 54 and 64, as reproduced above. This is because Blelloch fails to teach or suggest at least three features of these claims, and *In re Rose* does not make up for these deficiencies. Specifically, Blelloch fails to disclose (1) indices in an index vector that each select one data element, (2) independent selection of data elements by each index in the index vector and (3) provision of a data element selected by each index to a predetermined position in a destination register, as discussed in detail below.

**A.     Blelloch fails to disclose indices in an index vector in which each index selects one data element**

First, Blelloch fails to disclose indices in an index vector in which each index selects one data element. Blelloch discloses a “permute” operation that is fundamentally different from the present invention as recited in the claims. In Blelloch’s “permute” operation, an index vector identifies the *destination locations* to which data elements are to be sent. This is quite different from the use of indices such that each index selects the *data element* to be provided to a particular predetermined position in a destination register, as recited in the claims. An illustration of Blelloch’s “permute” operation is reproduced below (Blelloch at p. 62):

$$\begin{array}{rcl}
 \text{A (data vector)} & = & [a_0 \quad a_1 \quad a_2 \quad a_3 \quad a_4 \quad a_5 \quad a_6 \quad a_7] \\
 \text{I (index vector)} & = & [2 \quad 5 \quad 4 \quad 3 \quad 1 \quad 6 \quad 0 \quad 7] \\
 \\ 
 \text{C — permute(A, I)} & = & [a_6 \quad a_4 \quad a_0 \quad a_3 \quad a_2 \quad a_1 \quad a_5 \quad a_7]
 \end{array}$$

In this example, Blelloch’s index vector comprises the values [2 5 4 3 1 6 0 7]. The value “2” indicates that the first data element in a source vector is to be sent to the destination location “2.” The value “5” indicates that the next data element in the source vector is to be sent to the destination location “5,” and so on. Thus, each of these values in the index vector identifies the destination location where the particular data element is to be sent. These values do not select data elements, as is done in the claimed invention. Thus, Blelloch clearly fails to disclose the claimed feature of indices in an index vector in which each index selects one data element.

This difference between Blelloch and the present invention has important practical implications. By relying on the identification of destination locations (as opposed to selection of each data element), Blelloch’s permutation operation is necessarily restricted to a one-to-one

mapping. Indeed, the operation suffers from the risk of a potential error condition that would occur if two indices were accidentally given the same value, *i.e.*, same destination location. If that occurs, two different data elements would be headed to the same destination location, which causes a conflict. See Blelloch, p. 62, paragraph 3 (“It is an error for more than one element to contain the same index – a permutation is a one-to-one mapping. This restriction is similar to the restriction made in the exclusive-read exclusive-write (EREW) P-RAM model, in which it is an error to write more than one value to a particular memory location at a time”).

By contrast, the present invention utilizes an index vector comprising indices such that each index selects one data element to be provided to a predetermined position in the destination register. The design of the present invention is thus not limited to a one-to-one mapping. For example, if one index in the index vector selects a particular data element, another index in the index vector can select the same data element. In that case, the data element would be provided to two different predetermined positions in the result register. Clearly, this is not a one-to-one mapping and would not be achievable with Blelloch’s permutation operation. Furthermore, because the data element selected by each index is provided to its own predetermined position, the risk of accidental assignment of two data elements to the same destination location is completely eliminated. The technique of the present invention is fundamentally different from that of Blelloch and does not suffer from the potential of error conditions that are inherent in Blelloch’s permutation operation.

**B. Blelloch fails to disclose independent selection of a data element by each index in the index vector**

Second, Blelloch fails to disclose *independent* selection of a data element by each index in the index vector. In the presently claimed invention, each index in the index vector independently selects a data element from the plurality of data elements stored in the registers.

Blelloch fails to disclose this feature. As discussed previously, Blelloch's permutation operation is restricted to a one-to-one mapping that forbids two indices from selecting the same destination location. Each index can only select a destination location that is not selected by any other index. The value of one index is thus affected by, and affects, every other index in the index vector. Clearly, each index cannot independently select a destination location – it must make the selection in view of the selections made by the other indices to avoid selecting a destination location that has already been selected by another index.<sup>7</sup> Thus, not only does Blelloch fail to disclose selection of data elements as discussed previously (instead Blelloch discloses selection of destination locations), Blelloch also fails to disclose independent selection of a data element (or a destination location) by each index in its index vector. For this additional reason, Blelloch fails to disclose the presently claimed invention.

**C. Blelloch fails to disclose provision of a data element selected by each index to a predetermined position in a destination register**

Third, Blelloch fails to disclose provision of a data element selected by each index to a predetermined position in a destination register. Blelloch's permutation operation is specifically designed to allow the destination locations of the elements to be provided as an argument that can be varied during execution of the computer program that utilizes the operation. *See* Blelloch, p. 62, paragraph 2 (“The permute instruction takes two vector arguments – a data vector and an index vector – and permutes each element in the data vector to the location specified in the index vector”). By contrast, the claimed invention utilizes a different approach based on the selection of data elements, as opposed to destination locations, and the provision of selected data elements to predetermined positions within a destination register. Blelloch's teaching of a destination location that is variable during execution cannot be reasonably construed to constitute a

---

<sup>7</sup> Otherwise, two or more elements can be directed to the same destination location, which causes a conflict, as discussed.

“predetermined position” as recited in the claims. Accordingly, Blleloch fails to disclose the claimed feature of providing a data element selected by each index to a predetermined position in the destination register. For this yet additional reason, Blleloch fails to disclose the presently claimed invention.

The principles of *In re Rose* do not make up for the deficiencies of Blleloch. *In re Rose* includes a holding relating to the determination of obviousness when all of the elements of a claim are found in the cited prior art, and the only difference between the cited prior art and the claimed invention is a change in size. Here, the difference between Blleloch and the presently claimed invention is not merely a change in the size of the data. At least three claimed features of the present invention are missing from the disclosure of Blleloch, as discussed above. The absence of these claimed features from the Blleloch is not rendered obvious by merely changing the size of the data. Thus, applying the holding of *In re Rose* to Blleloch fails to render obvious many of the features of the claimed invention.

For at least the reasons stated above, Applicants assert that claims 40, 50, 54, and 64 are patentable over Blleloch in view of the *In re Rose* holding. Claims 48, 51-53, 62, and 63-67 depend from claims 40, 50, 54 and 64, respectively, and incorporate all the limitations of their respective base claims. As such, claims 48, 51-53, 62, and 63-67 are also patentable over Blleloch in view of the *In re Rose* holding for at least the reasons stated above with respect to claims 40, 50, 54, and 64. Accordingly, Applicants respectfully request withdrawal of the rejection based in Blleloch in view of *In re Rose*.

## VI. STATEMENT REGARDING KSR AND OBVIOUSNESS IN GENERAL

Having addressed the specific obviousness rejections based on Lee in view of Matsuura and based on Blleloch in view of *In re Rose*, Applicants now turn to the Office Action's citation of *KSR v. Teleflex*, 550 U.S. 398 (2007) and its general statement alleging that all elements necessary to the claimed invention, as well as how one would combine such elements, "were known in the art." See Office Action, pp.13-14.

With regard to the citation of *KSR*, Applicants respectfully submit that the holding of this case does not render the pending claims unpatentable as set forth in the Office Action. While *KSR* addresses the proper standard for combining prior art references, it does not remove the requirement that all claimed elements must still be disclosed when the cited prior art is combined. As the Board of Patent Appeals and Interferences held in a recent post-*KSR* decision, a proper obviousness determination requires that an Examiner make "a searching comparison of the claimed invention - *including all its limitations* - with the teaching of the prior art." See *In re Wada and Murphy*, Appeal 2007-3733, citing *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis in original). As Applicants have explained above, even if the cited prior art references were combined, the resulting combination would not disclose all of the elements of the claimed invention.<sup>8</sup> Because *KSR* does not remove the requirement that obviousness must be established by a showing that all claimed elements are disclosed when the prior art is combined, the holding in *KSR* cannot be relied upon to establish obviousness of the claimed inventions.

---

<sup>8</sup> With respect to the rejection based on Lee in view of Matsuura, Applicants have submitted detailed declaration under 37 C.F.R. § 1.131 disqualifying the Lee patent. The only prior art reference that remains, Matsuura, fails to disclose all of the limitations of the rejected claims. See section IV above. With respect to the rejection based on Blleloch in view of *In re Rose*, Applicants explained in detail how the combination of Blleloch and *In re Rose* fails to disclose all of the elements of the rejected claims, as amended. See section V above.

The Office Action also included a statement alleging that all elements necessary to the claimed invention and how one would combine such elements “were known in the art.” The Office Action states, at p. 14:

All the elements necessary to produce the applicants’ invention were known in the art. How one combined such elements to produce applicants’ invention was also known in the art. Evidence of this is that applicants’ disclosure lacks any detailed description of unique technology necessary to implement applicants’ invention. One of ordinary skill would have readily recognized that the results of the combination were predictable. Absent some secondary considerations, not in evidence at this time, applicants invention is obvious over the combination of prior art presented.

To the extent that this statement is intended as an additional rationale for obviousness, Applicants respectfully submit that such a statement is not merely incorrect and unsupported, it is also too vague, and thus it is difficult to provide a meaningful response. An obviousness rejection must be articulated specifically and not as a general allegation. As the MPEP puts it, at § 2142:

The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR International Co. v. Teleflex Inc.*, 550 U.S. [], 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that “rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). See also *KSR*, 550 U.S. at [], 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval)

Applicants have set forth herein detailed responses to the specific obviousness rejections presented in the Office Action – Lee in view of Matsuura, as well as Bieleloch in view of *In re Rose*. However, Applicants cannot respond meaningfully to a general allegation that elements of the invention and how one would combine them “were known in the art.” As such, Applicants believe proper responses have been submitted herein to all pending obviousness rejections.



However, if there are any grounds for obviousness rejections that have not been fully addressed, the PTO is invited to discuss such grounds with Applicants either in the next Office Action or by telephone with the Applicants' representative.<sup>9</sup>

**CONCLUSION**

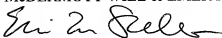
In view of the above remarks, Applicants respectfully submit that the application is in condition for allowance, and respectfully request the Examiner's favorable reconsideration as to allowance. The Examiner is invited to contact the Applicants' representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

*Attachment: Exhibits 1-6*

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Eric M. Shelton

Registration No. 57,630

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
Phone: 202.756.8000 EMS:MWE  
Facsimile: 202.756.8087  
**Date: January 8, 2009**

**Please recognize our Customer No. 20277  
as our correspondence address.**

---

<sup>9</sup> Applicants reserve the right to submit appropriate evidence of secondary indicia of nonobviousness. The claims have been amended and include elements not found in the cited prior art references, even if the references are combined. Thus, a prima facie case of obviousness has not been established with regard to the amended claims, and a demonstration of secondary considerations would be inappropriate at this time.